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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,838	BAILEY ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 were examined.

Section I: Continued Prosecution Application

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/07/2005 has been entered.

Section II: Non-Final Rejection (3rd Office Action)

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-5, 7-20,22-29,32,34,35,37 are rejected under 35 U.S.C. 103 (a) as unpatentable by Klein et al. (U.S. Patent 5,768,567 (1998)), (hereafter Klein) in view of Rajsuman et al. (U.S. Patent 6,678,645 (2004)) (Rajsuman). Klein and Rajsuman are analogous art because they both teach hardware-software co-simulation with C++ or HDL language.

At the time of invention, it would have been obvious to one of ordinary skill in the art to utilize the optimizing hardware-software co-simulation of Klein in the system-on-

chip validation of Rajsuman because Rajsuman teaches high speed, low cost SoC design validation (Rajsuman: column 4, lines 52-55).

Claim 1 . A method comprising: selectively activating and deactivating particular simulation domains (Klein: column 17, lines 1-5) in a simulation environment such that a resolution and a performance (Rajsuman: column 5, 34-41) for a circuit design being simulated is dynamically modified (Klein: column 3, lines 1-5); and said simulation environment comprising a plurality of simulation domains (Klein: column 14, lines 16-24).

Claim 2. The method of claim 1 wherein the plurality of simulation domains comprises at least one of a software execution domain (Rajsuman: column 12, lines 21-25) a hardware simulation domain, and an abstract model simulation domain.

Claim 3. The method of claim 2 wherein the software execution domain comprises at least one of a native processor package (specification notes native processor as simulation clock—Klein: column 16, lines 35-40), an instruction set simulator (ISS) (Klein: column 2, lines 55-60), and a programming language simulator (Rajsuman: column 12, lines 21-25) to model software execution in one or more processors.

Claim 4. The method of claim 2 wherein the hardware simulation domain comprises (Klein: column 2, lines 55-60) at least one of a logic simulator and a programming language simulator (Rajsuman: column 12, lines 21-25).

Claim 5. The method of claim 4 wherein the logic simulator comprises one of a hardware description language (HDL) based simulator (Rajsuman: column 12, lines 21-25), a gate-level simulator (Rajsuman: column: 11, lines 4-11 with Klein: column 2, lines 55-60), a simulation accelerator, a system simulator, a cycle simulator, and a programmable hardware emulator (Rajsuman: column 12, lines 21-25).

Claim 7. The method of claim 1 wherein each of the plurality of simulation domains comprises at least one model of a circuit element in the circuit design (Rajsuman: column 13, lines 55-60).

Claim 8. The method of claim 1 further comprising: partitioning the circuit design into the plurality of simulation domains (Rajsuman: column 13, lines 55-60) based on a partition (Klein: column 15, line 42) criteria.

Claim 9. The method of claim 8 wherein the partition (Klein: column 15, line 42) criteria comprises at least one of an abstraction level, (Rajsumann: column 3, lines 45) a simulation type, and a function type (Rajsumann: column 3, lines 36, 45 and 51).

Claim 10. The method of claim 9 wherein partitioning the circuit design based on the abstraction level partitions (Klein: column 15, line 42 with Rajsuman: column 1, lines 50-55) the circuit design into at least one of a pin-level domain (Rajsuman: column 13, lines 34), a bus-level domain (Rajsuman: column 2, lines 41-47) and a transaction-level domain.

Claim 11. The method of claim 9 wherein partitioning the circuit design based (Klein: column 15, line 42) on the simulation type partitions the circuit design into at least one of a software execution domain, a logic simulator domain, and a programming language simulator domain (Rajsuman: column 1, lines 37-40).

Claim 12. The method of claim 9 wherein partitioning the circuit design (Klein: column 15, line 42) based on the function type comprises: identifying one or more functional elements in the circuit design that have a particular level of independent operation from the remainder of the circuit design (Rajsuman: column 2, lines 40-55); and defining a domain encompassing each identified functional element (Rajsuman: column 2, lines 40-55).

Claim 13. The method of claim 1 wherein each of the plurality of simulation domains provides a particular performance level and a particular resolution level, ("abstraction levels" Rajsuman: column 2, lines 16-20) and wherein the particular simulation domains (Klein: column 3, lines 1-5) are selectively activated or deactivated during particular

stages of simulation in combinations that either accelerate performance of the simulation environment or increase resolution of the simulation environment.

Claim 14. The method of claim 1wherein selectively activating and deactivating the particular simulation domains (Klein: column 3, lines 1-5) comprises: identifying a system state of the circuit design; determining which of the plurality of simulation domains are to be active for the identified system state (Klein: column 3, lines 14-24); and advancing simulation time only in each activated simulation domain (Klein: column 3, lines 1-5).

Claim 15. The method of claim 14 wherein determining which of the plurality of simulation domains (Klein: column 3, lines 1-5) are to be active for the identified system state comprises at least one of a centralized control, a transaction-based control (Klein: columns 10-11, lines 57-67, 1-11, respectively) and a distributed control.

Claim 16. The method of claim 15 wherein the centralized control comprises: receiving the system state from one or more of the plurality of simulation domains (Klein: column 3, lines 1-5) consulting system configuration information to determine which of the plurality of simulation domains correspond to the particular system state (Klein: column 5, lines 56-67); and instructing a centralized simulation clock (Klein: column 3, lines 14-20) to advance only for those domains corresponding to the particular system state.

Claim 17. The method of claim 15 wherein the system state comprises system addresses (Klein: column 3, lines 30-37) in the circuit design.

Claim 18. The method of claim 15 wherein the system state comprises a data transaction in the circuit design, said data transaction being configured with information identifying which of the plurality of simulation domains are to be active for the data transaction, and wherein the transaction-based control comprises: sending a message to centralized simulation clock as part of the data transaction, said message to instruct the centralized simulations clock (Klein: column 3, lines 14-20) with respect to which of the plurality of simulation domains (Klein: column 3, lines 1-5) are to be for the data transaction.

Claim 19. The method of claim 15 wherein a predetermined simulation domain (Klein: column 3, lines 1-5) is configured with activation information identifying at least one particular system state for which the predetermined simulation domain is to be active, (Klein: column 3, lines 14-20) wherein identifying the system state comprises receiving a broadcast of the system state at the predetermined simulation domain, (Klein: column 3, lines 1-5) and wherein distributed control at the predetermined simulation domain comprises: determining if the predetermined simulation domain is to be active for the identified system state based on the activation information (Klein: columns 2 and 3, lines 55-67, 1-14, respectively); and advancing an operation in the predetermined simulation domain accordingly (operator driven i.e., inherent).

Claim 20. The method of claim 19 wherein the information further identifies an event for terminating operation of the predetermined simulation domain (Klein: column 11, lines 24-27) for the at least one particular system state.

Claim 22. The method of claim 1 wherein the plurality of simulation domains (Klein: column 3, lines 1-5) comprises a hierarchical structure, and wherein selectively activating and deactivating (operator /user driven) the particular simulation domains on levels of the hierarchical structure.

Claim 23. The method of claim 1 wherein each of the plurality of simulation domains comprises at least one simulation model, the method further comprising: identification state information comprising a transfer from a first simulation model in the simulation environment, said transfer being directed to a second simulation model in a circuit design being simulated in the simulation environment; receiving the state information from the first simulation model (Rajsuman: column 4, lines 1-6); and making the state information available to the second simulation model without simulating the transfer in the circuit design (Klein: column 10, lines 14-16).

Claim 24. The method of claim 23 wherein simulating the transfer from the first simulation model to the second simulation model in the circuit design comprises

transferring the state information through at least one additional simulation model in the simulation environment.

Claim 25. The method of claim 23 wherein receiving the state information and making the state information available comprises: storing the state information in a coherent state memory space that is part of the simulation environment and corresponds to an element in the circuit design being simulated (Klein: column 18, lines 40-46), said coherent state memory space being accessible to both the first simulation and the second simulation model.

Claim 26. The method of claim 25 wherein the coherent state memory space is accessible to a plurality of additional simulation models.

Claim 27. The method of claim 23 wherein receiving the state information and making the state information available comprises at least one of: a virtual transfer path (as defined in the specification as where a simulation model does not exist for a particular data path in the circuit design—coherent memory: Klein: column 18, lines 40-45) for use when a simulation model of a transfer path in the circuit design is not included in the simulation environment; and a higher performance (not addressed: speculative/opinion) transfer path than the simulation model of the transfer path in the circuit design.

Claim 28. The method of claim 27wherein the higher performance transfer path provides a lower level of resolution than the simulation model of the transfer path in the circuit design.

Claim 29. The method of claim 1 (Klein: column 17, lines 1-5; Rajsuman: column 5, 34-41; column 14, lines 16-24) wherein a first simulation model and a second simulation model of the plurality of simulation models represent different versions of a same functionality in the circuit design.

Claim 32. The method of claim 1 wherein a set of simulation models among a plurality of simulation models represent a same functionality in the circuit design, each of the set of the set of simulation models being used at different stages of simulation depending on a desired performance level and/or resolution level of the simulation.

Claim 34. The method of claim 23 wherein both the first simulation model and the second simulation model are within a same simulation domain in the simulation environment.

Claim 35. The method of claim 23 wherein the first simulation model and the second simulation model are within different simulation domains in the simulation environment.

Claim 37. The method of claim 2 wherein the abstract model simulation domain comprises at least one of a hardware description language (HDL) simulator and a programming language simulator (Rajsuman: column 12, lines 1-25).

6. Claims 6, 36 and 38 are rejected under 35 U.S.C. 103 (a) as unpatentable by Klein et al. (U.S. Patent 5,768,567 (1998)), in view of Rajsuman (U.S. Patent 6,678,645 (2004)) in further view of Barnett et al. (U.S. Patent 6,223,144 (2001)). Klein, Rajsuman and Barnett are analogous art because each of them teaches high level programming languages.

At the time of invention, it would have been obvious to one of ordinary skill in the art to utilize the optimizing hardware-software co-simulation of Klein in the system-on-chip validation of Rajsuman and the microcontroller simulation function of Barnett because Rajsuman and Barnett teach high speed, low cost SoC design validation (Rajsuman: column 4, lines 52-55) and a low cost system for testing and debugging software by a programmer at compile time (Barnett: column 3, lines 11-14).

Claim 6. The method of claim 4 wherein the programming language simulator comprises at least one of a C programming language simulator, a C++ programming language simulator, a simulator using a C-based language, a simulator using a C++ based language, and a JAVA programming language simulator (Barnett: column 4, line 19).

Claim 36. The method of claim 3 wherein the programming language simulator comprises at least one of a C programming language simulator, a C++ programming language simulator, a simulator using a C-based language, a simulator using a C++ based language, and a JAVA programming language simulator (Barnett: column 4, line 19).

Claim 38. The method of claim 37 wherein the programming language simulator comprises at least one of a C programming language simulator, a C++ programming language simulator, a simulator using a C-based language, a simulator using a C++ based language, and a JAVA programming language simulator (Barnett: column 4, line 19).

7. Claims 21 is rejected under 35 U.S.C. 103 (a) as unpatentable by Klein et al. (U.S. Patent 5,768,567 (1998)), in view of Rajsuman et al. (U.S. Patent 6,678,645 (2004)) in further view of Rush (U.S. Patent 5,742,181 (1998)). Klein, Rajsuman and Rush are analogous art because each of them teaches high level programming languages.

At the time of invention, it would have been obvious to one of ordinary skill in the art to utilize the optimizing hardware-software co-simulation of Klein in the system-on-chip validation of Rajsuman and the simulation and emulation of FPGAs with hierarchical structure of Rush because Rajsuman and Rush teach high speed, low cost SoC design validation (Rajsuman: column 4, lines 52-55) and the verification can

greatly decrease the amount of time that is required to design an ASIC so long as the FPGA can be quickly configured to functionally emulate the ASIC design (Rush: column 1, lines 23-26).

Claim 21. The method of claim 14 wherein determining which of the plurality of simulation domains are to be active for the identified system state depends on a plurality of control mechanisms, wherein each of the plurality of control mechanisms comprises a priority level, and wherein a higher priority control mechanism takes precedence over a lower priority control mechanism.

8. Claims 30,31, and 33 are rejected under 35 U.S.C. 103 (a) as unpatentable by Klein (U.S. Patent 5,768,567 (1998)), in view of Rajsuman (U.S. Patent 6,678,645 (2004)) in further view of Patel (U.S. Patent 5,546,562 (1996)). Klein, Rajsuman and Patel are analogous art because each one of them teaches hardware-software simulation.

At the time of invention, it would have been obvious to one of ordinary skill in the art to utilize the optimizing hardware-software co-simulation of Klein in the system-on-chip validation of Rajsuman and the state information of Patel because Rajsuman teaches high speed, low cost SoC design validation (Rajsuman: column 4, lines 52-55) and to provide tremendous savings in debugging effort (Patel: column 4, line 48).
Claim 30. The method of claim 29 further comprising: simulating the circuit design using the first simulation model, said first simulation model to generate state information

(Patel: column 8, lines 30-35); and switching to simulate the circuit design using the second simulation model (Klein: column 22, lines 10-15), said first simulation model to transfer the state information (Patel: column 8, lines 30-35) to the second simulation model prior to the second simulation model being used.

Claim 31. The method of claim 30 wherein the first simulation model and the second simulation model each have a particular level of performance and resolution, and wherein switching to the second simulation model (Klein: column 22, lines 10-15) is based on a change in a performance level and/or a resolution level desired at a different stage of simulation.

Claim 33. The method of claim 25 wherein the simulation environment comprises a plurality of additional simulation models, each of the plurality of additional simulation models corresponding to one or more of a plurality of additional coherent state memory spaces, the method further comprising: identifying additional state information (Patel: column 8, lines 30-35) comprising additional transfers among the plurality of additional simulation models in the simulation environment; and storing the additional state information in appropriate ones of the plurality of additional coherent state memory (as defined in the specification as where a simulation model does not exist for a particular data path in the circuit design—coherent memory: Klein: column 18, lines 40-45) space such that the additional state information is accessible to corresponding ones of the

plurality of additional simulation models without simulating the additional transfers in the circuit design.

9. Claims 39 and 40 are rejected under 35 U.S.C. 103 (a) as unpatentable by Fordham et al., US Patent 5,136,528. (Hereafter Fordham) in view of Oydryna et al., "A Workstation-Mixed Model Circuit Simulator" (hereafter Odryna). Fordham and Oydryna are analogous art since both of them teach simulation of circuits.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize the timing simulation algorithm of Odryna in the controller means of Fordham because Odryna teaches reducing the amount of CPU time and CPU memory used so that single-user workstations such as the 68010 based SUN-2 and Apollo systems can be used interactively. Designers' use of this simulator has indicated that circuit problem diagnosis and performance estimation has become as easy as the rest of the design task (Odryna: pg. 192, left column, "Summary" section, last paragraph).

Claim 39: A machine readable storage medium (Odryna: pg. 187, right column, 1st paragraph "CPU") having stored thereon machine readable instructions that when executed implement a method comprising: selectively activating and deactivating particular simulation (Fordham: column 2, lines 20-25) domains in a simulation environment such that a resolution and a performance for a circuit design (Odryna: pg. 191, "Design Optimization" section) being simulated can be dynamically modified; and said simulation environment comprising a plurality of simulation domains (Odryna: pg. 188, left column, 4th paragraph).

Claim 40. The machine readable storage medium of claim 39, wherein the method further comprises partitioning the circuit design into the plurality of simulation domains based on partition criteria (Odryna: pg. 187, right column, 2nd paragraph, lines 3-9).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

March 15, 2006

TS

Paul L. Rodriguez 3/15/06
Primary Examiner
Art Unit ~~2125~~ 2123